

CLAIMS

What is claimed is:

- 1 1. An integrated circuit chip package comprising:
 - 2 a metal substrate core including,
 - 3 a first region, and
 - 4 a second region electrically isolated from the first region.
- 1 2. The integrated circuit chip package of claim 1, wherein at least one of the regions
2 of the substrate core is coupled with an operating voltage rail of an integrated circuit chip.
- 1 3. The integrated circuit chip package of claim 1, wherein at least one of the regions
2 of the substrate core is coupled with a digital ground of an integrated circuit chip.
- 1 4. The integrated circuit chip package of claim 1, wherein at least one of the regions
2 of the substrate core is coupled with an analog ground of an integrated circuit chip.
- 1 5. The integrated circuit chip package of claim 1, wherein at least one of the regions
2 of the substrate core is coupled with an operating voltage rail of an integrated circuit chip,
3 and at least one other of the regions of the substrate core is coupled with a digital ground
4 of the integrated circuit chip.

1 6. The integrated circuit chip package of claim 1, wherein at least one of the regions
2 of the substrate core is coupled with an operating voltage rail of an integrated circuit chip,
3 and at least one other of the regions of the substrate core is coupled with an analog
4 ground of the integrated circuit chip.

1 7. The integrated circuit chip package of claim 1, wherein at least one of the regions
2 of the substrate core is coupled with a digital ground of an integrated circuit chip, and at
3 least one other of the regions of the substrate core is coupled with an analog ground of the
4 integrated circuit chip.

1 8. An integrated circuit chip package comprising:
2 a metal substrate core;
3 the metal substrate core having at least two electrically isolated regions;
4 wherein at least one of the electrically isolated regions of the metal substrate core
5 is coupled with a digital ground of an integrated circuit chip.

1 9. The integrated circuit chip package of claim 8, further comprising:
2 input and output signals of the integrated circuit chip routed through the
3 electrically isolated region of the metal substrate core that is coupled with the digital
4 ground of the integrated circuit chip.

1 10. The integrated circuit chip package of claim 9, wherein at least one other of the
2 electrically isolated regions of the metal substrate core is coupled with an operating
3 voltage rail of the integrated circuit chip.

1 11. The integrated circuit chip package of claim 9, wherein at least one other of the
2 electrically isolated regions of the metal substrate core is coupled with an analog ground
3 of the integrated circuit chip.

1 12. An integrated circuit chip package comprising:
2 a metal substrate core;
3 the metal substrate core having at least three electrically isolated regions;
4 wherein at least one of the electrically isolated regions of the metal substrate core
5 is coupled with a digital ground of an integrated circuit chip and has input and output
6 signals routed through it.

1 13. The integrated circuit chip package of claim 12, wherein at least one other of the
2 electrically isolated regions of the metal substrate core is coupled with an operating
3 voltage rail of the integrated circuit chip.

1 14. The integrated circuit chip package of claim 12, wherein at least one other of the
2 electrically isolated regions of the metal substrate core is coupled with an analog ground
3 of the integrated circuit chip.

1 15. The integrated circuit chip package of claim 12, wherein at least one other of the
2 electrically isolated regions of the metal substrate core is coupled with an operating
3 voltage rail of the integrated circuit chip, and at least one other of the electrically isolated
4 region of the metal substrate core is coupled with an analog ground of the integrated
5 circuit chip.

1 16. A method comprising:
2 creating initial clearances on a metal substrate core that do not fully electrically
3 separate the core into two ore more regions;
4 filling the initial clearances with dielectric material; and
5 creating final clearances that fully electrically separate the two or more regions of
6 the metal substrate core.

1 17. The method of claim 16, further comprising filling the final clearances with
2 dielectric material.

1 18. The method of claim 16, wherein creating the initial or final clearances comprises
2 chemical etching.

1 19. The method of claim 16, wherein creating the initial or final clearances comprises
2 laser etching.

- 1 20. The method of claim 16, wherein creating the initial or final clearances comprises
2 mechanical methods including at least one of drilling, routing, and punching.

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